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10/760,659	01/20/2004	Simon C. Steely JR.	200313629-1	9866

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EXAMINER	
CHERY, MARDOCHEE	
ART UNIT	PAPER NUMBER
2188	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/760,659	STEELY ET AL.	
	Examiner	Art Unit	
	Mardochee Chery	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,8-12 and 18-32* is/are rejected.

7)☒ Claim(s) *2-7,13-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to Applicant's communication filed on January 30, 2007 in response to PTO Office Action mailed on November 17, 2006. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. Claims 1-32 remain pending.

Response to Arguments

3. Applicant's arguments filed January 30, 2007 have been fully considered but they are not persuasive.

a. Applicants argue on page 12 of the remarks that Arimilli fails to teach that "the second node is operative to receive data from the first node and that the second node is operative to assign a shared state to an associated state of the data at the second node", recited in claim 1.

i. Examiner strongly disagrees. Arimilli clearly discloses "master 26 of a first agent, for example, processor complex 10a, issues modifying transaction 150a on system bus 12 that targets a cache line that is indicated as shared in the cache directory 22 of at least one agent 10; a result of a store request by the processor 16 in the second agent 10 that

targets a cache line marked as shared in the second agent's cache processor 22; par. [0029]."

ii. Chen further discloses "at least a first and a second nodes; the first node includes an external cache for storing a data from a local memory of the second node and at least two processors optionally accessing the data from the external cache; whether a second certain one of at least two processors is allowed to share the modified data is further determined; if the second certain processor is allowed to share the modified data, it may directly request the modified data from the first certain processor; Abstract".

b. Applicants argue on page 13 of the remarks that none of the cited sections of Chen, nor Chen more generally, teach or suggest that a first node is operative to do any action, let alone to provide the data to the second node and transition the associated state of the data at the first node from the modified state to an owner state in response to a non-migratory source broadcast request provided by the second node.

Examiner strongly disagrees with such contention. As described on pages 5, 8, of applicants' disclosure "a protocol employs a dirty (D-state) and an owner-shared state (O-state) to enable read migration without updating memory; the inclusion of the D-state and O-state in the cache coherency protocol allows for migration of data, without write-back, when requested from a cache containing the data in the M-state". Further, on page 8,

paragraph [0037] to page 9, paragraph [0039] provides instances where "a first node in response to a non-migratory source broadcast request provides data to a second node and transition an associated state of the data at a first node from modified state to an owner state without updating memory", namely:

[0037] Upon receiving the data from the target processor 14, the source processor 12 places the data in the appropriate cache line in its cache 22. The source processor 12 transitions the cache line of the cache 22 from the I-state to the D-state. In the D-state, the source processor 12 has the most up-to-date version of the data stored in its cache 22 and has not modified the data (e.g., by writing to the cache line in the cache 22). The data has thus migrated from the target processor 14 to the source processor 12 without write-back to (updating) the memory 16. Additionally, the D-state defines the processor 12 as a new cache ordering point for the data.

[0038] Continuing with the above example, assume that a processor (e.g., processor 14) broadcasts a migratory read request (XREADM) for the data, which is stored in the D-state in cache 22 of processor 12, as may occur after the initial read migration described above. The source processor 14 broadcasts an XREADM request to all other processors in the system 10, including the target processor 12 and those located in the other nodes 20, as well as to the memory 16. If the target processor 12

has not modified (e.g., written) the data, the target processor responds by providing a shared data response to the source processor 14 and transitioning the target processor cache line associated with the data from the D-state to the O-state. The requested data is received at the source processor 14 and placed in the appropriate cache line in the source processor cache 24. The source processor 14 cache line transitions from the I-state to the S-state because, at this point, an up-to-date copy of the data is shared by both the source processor 14 (S-state) and the target processor 12 (O-state). Migration from the target processor 12 to the source processor 14 has not occurred because the target had not modified the data at the time of the XREADM request.

[0039] In the S-state, the source processor 14 has a valid and unmodified copy of the data. Since other processors may have valid copies of the data, the source processor 14 (being in the S-state) cannot respond to snoops by returning data and cannot write-back the data to memory 16. In the O-state, the target processor 12 has the most up-to-date version of the data stored in its cache 22. The target processor 12 cannot modify the data, and must write-back the data to memory 16 upon displacement (e.g., upon a write request or invalidate issued by another node). The target processor 12, being in the O-state, can respond to read requests by returning shared data, and thus may respond to subsequent read requests from other processors.

Similarly, Chen unequivocally discloses "the data in the cache has been modified and exclusively owned by a certain processor of the local node, and thus has become different from that existing in the home node; a command is issued to read an exclusive copy of the specific data which is stored in the local node and has not been modified, or read an exclusive copy of the specific data which is stored in the local node and has been modified, or modify a shared copy of the specific data and exclusively own the specific data; changing the state of the local memory line of the remote node where the specific data is stored, from GONE into HOME, or changing the state of the local memory line of the remote node, from SHARED to HOME; col. 5, ll 5-10, 36-42; col. 5, ll 60 to col. 6, ll 6." Chen further discloses "discriminating whether the data has been modified by a first certain one of the at least two processors on the condition that a cache line of the external cache, where the data is stored, is in a CLEAN state; changing the state of the cache line from the CLEAN state to either of DIRTY-SHARED and DIRTY-ONLY state if the data has been modified into a modified data and allowing a second certain one of the at least two processors to directly request the modified data via a bus inside the first node when the cache line is in the DIRTY_SHARED state; col. 3, ll 55-65; In CLEAN state, when the processor 112 is going to read and modify the exclusive copy of the data in the cache line, if the data is in the cache 1141 but has been modified, the modified data in the cache line, which

becomes different from the data stored in the local memory 1231 of the home node 12, will be directly read off the bus 115 and exclusively owned by the processor 112, and thus the state of the cache line changes from CLEAN to DIRTY-ONLY; in CLEAN state, when the processor 112 is going to get a shared copy of the data in the cache line, and permits another processor to share the data...if the data is in the cache 1141 but has been modified...the modified data in the cache line, which becomes different from the data stored in the local memory 1231 of the home node 12, will be directly read off bus 115 by the processor 112 and shared with other processors, and thus the state of the cache line changes from CLEAN to DIRY-SHARED; col. 6, ll 48 to col. 7, ll 2."

Thus, Chen clearly discloses, in the manner described in applicants' disclosure, "a protocol employs a dirty (D-state) and an owner-shared state (O-state) to enable read migration without updating memory; the inclusion of the D-state and O-state in the cache coherency protocol allows for migration of data, without write-back, when requested from a cache containing the data in the M-state, and as such discloses "a first node in response to a non-migratory source broadcast request provides data to a second node and transition an associated state of the data at a first node from modified state to an owner state without updating memory".

c. Applicants argue on page 14, paragraph 1 of the remarks that "Chen fails to disclose a source broadcast system so the system is not operative to respond to source broadcasts, allegedly recited in claim 8.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., disclose a source broadcast system so the system is not operative to respond to source broadcasts) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

d. Applicants argue on page 14, paragraph 2 of the remarks that the Abstract of Arimilli fails to state that "after the first node shares the data to the second node that further migration of the data is precluded when the associated state of the data at the second node is share data", allegedly recited in claim 9.

Examiner would like to emphasize that claim 9, simply states "...wherein further migration of the data from the second node is precluded when the associated state of the data at the second node is the shared state". Examiner would like to further point out that Applicant is reading limitations of the specification into the claims to thereby narrow the scope of the claims by implicitly adding disclosed limitations which have no express basis in the claims. This is impermissible importation of

subject matter from the specification into the claim and such is not in accordance with USPTO rules and procedures. See MPEP 2111. See also *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997).

e. Applicants argue on page 14, paragraph 3 of the remarks that Chen fails to teach or suggest a relationship between three nodes: first, second and at least one other node – and also fails to teach a system with source broadcast requests", allegedly recited in claim 10.

Examiner would like to point out that Applicant is reading limitations of the specification into the claims to thereby narrow the scope of the claims by implicitly adding disclosed limitations which have no express basis in the claims. This is impermissible importation of subject matter from the specification into the claim and such is not in accordance with USPTO rules and procedures. See MPEP 2111. See also *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997).

f. Applicants' arguments on page 15, with respect to claim 12 are identical to arguments presented on page 12, with respect to claim 1. As such, the paragraphs supra addressing those arguments are herein referenced.

g. Applicants argue on page 16 of the remarks that Chen and Arimilli do not teach how the second cache controller is effecting state transitions associated with the data based upon data request and responses for the associated cache of the second processor", recited in claim 11.

Examiner strongly disagrees. Chen discloses, at least in Figs 2-5 how cache states are transitioned where it is readily apparent that such transitions result from data requests and responses of another node; "data in cache line is modified by certain processor; other processor may share modified data; another processor directly requests modified data; modified data is exclusively owned by certain processor; data in cache line is modified, and cache line changes from 1st to 2nd status; local memory line is in transition status; cache line recovers fro m2nd to 1st status; Fig.5."

h. Applicants' arguments on page 17, with respect to claim 21 are identical to arguments presented on page 16, with respect to claim 11. As such, the paragraphs supra addressing those arguments are herein referenced.

i. In view of the foregoing, it has been shown that the claimed invention is not patentably distinct over the combination of Arimilli (2002/0129211), Chen (6,931,496), and Cypher (6,484,240), when interpreted in light of the specification. Additionally, applicants should eschew reading limitations of the specification into the claims and holding the cited art to the ipsissimis verbis test,

i.e., identity of terminology is not required. Furthermore, in response to the Office action, applicants are advised to carefully study and review the cited art of record, and amend the claims to further compact prosecution. Hence the rejection of claims 1, 8-12, and 18-32 is strictly maintained.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 8-10, 12, 18-19, and 24-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli (2002/0129211) in view of Chen (6,931,496).

As per claim 1, Arimillli discloses a system comprising: a first node including data having an associated state, the associated state of the data at the first node being a modified state [page 7]; and a second node operative to provide a non- migratory source broadcast request for the data, the second node being operative to receive the data from the first node and assign a shared state to an associated state of the data at the second node [page 7].

However, Arimillli does not explicitly teach the first node being operative in response to the non-migratory source broadcast request to provide the data to the second node and to transition the associated state of the data at the first node from the modified state to an owner state without updating memory as required by the claim.

Chen discloses the first node being operative in response to the non-migratory source broadcast request to provide the data to the second node and to transition the associated state of the data at the first node from the modified state to an owner state without updating memory [col.5, ll 5-10, ll 36-42, ll 60 to col. 6, ll 6] to provide a data maintenance method in a distributed shared memory system to efficiently solve the access deadlock problem (col. 3, ll 10-12).

Since the technology for implementing a cache coherency system with transitioning the associated state of the data at the first node from the modified state to an owner state without updating memory was well known as evidenced by Chen, an artisan would have been motivated to implement this feature in the system of Arimillli to provide a data maintenance method in a distributed shared memory system to efficiently solve the access deadlock problem. Thus, it would have obvious to one of ordinary skill in the art at the time of invention by Applicant, to modify the system of Arimillli to include transitioning the associated state of the data at the first node from the modified state to an owner state without updating memory because this would have provided a data

maintenance method in a distributed shared memory system to efficiently solve the access deadlock problem (col. 3, ll 10-12) as taught by Chen.

As per claim 8, Chen discloses the first node is operative in response to the non-migratory source broadcast request to provide a shared data response to the second node [col. 6, ll 1-6].

As per claim 9, Arimillli discloses further migration of the data from the second node is precluded when the associated state of the data at the second node is the shared state [Abstract].

As per claim 10, Chen discloses at least one other node that provides a non-data response to the second node in response to the non-migratory source broadcast request from the second node, the non-data response indicating that the at least one other node does not have a valid copy of the data requested by the second node [col. 7, ll 55-61].

As per claim 12, the rationale in the rejection of claim 1 is herein incorporated.

As per claim 18, the rationale in the rejection of claim 9 is herein incorporated.

As per claim 19, the rationale in the rejection of claim 10 is herein incorporated.

As per claims 24 and 25, the rationale in the rejection of claim 1 is herein incorporated.

As per claim 26, Chen discloses means for selecting one of the XREADM request and XREADN request to broadcast from the first node [Figs. 4 and 5].

As per claim 27, Chen discloses means for predictively selecting one of the XREADM request and XREADN request to broadcast from the first node [Figs. 4 and 5].

As per claim 28, the rationale in the rejection of claim 1 is herein incorporated.

As per claim 29, the rationale in the rejection of claim 1 is herein incorporated.

As per claim 30, the rationale in the rejection of claim 26 is herein incorporated.

As per claim 31, the rationale in the rejection of claim 27 is herein incorporated.

As per claim 32, the rationale in the rejection of claim 1 is herein incorporated.

6. Claims 11 and 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimillli (2002/0129211) in view of Chen (6,931,496) and further in view of Cypher (6,484,240).

As per claim 11, Arimillli discloses the first node defines a first processor and the second node defines a second processor [Fig. 1], the first and second processors each having an associated cache that comprises a plurality of cache lines [Fig. 1], the first and second processors being capable of communicating with each other and with a system memory via an interconnect [Fig. 1, System Bus 12].

Chen further discloses the system further comprising a first cache controller associated with the first processor and a second cache controller associated with the second processor [Fig. 1], the first cache controller being operative to manage data requests and responses for the associated cache of the first processor [Fig. 1], the first cache controller effecting state transitions associated with the data in the associated cache of the first processor based on the data requests and responses for the associated cache of the first processor [Fig. 1], the second cache controller being operative to manage data requests and responses for the associated cache of the second processor [Fig. 1], the second cache controller effecting state transitions associated with the data in the associated cache of the second processor based on the data requests and responses for the associated cache of the second processor [Figs. 2-5].

However, Arimilli and Chen do not explicitly teach each cache line having a respective tag address that identifies associated data and each cache line having state information that indicates a state of the associated data for the respective cache line as required by the claim.

Cypher discloses each cache line having a respective tag address that identifies associated data and each cache line having state information that indicates a state of the associated data for the respective cache line [col. 1, ll 20-25] to specify the access rights and ownership responsibilities for a corresponding processor (col. 1, ll 23-25).

Since the technology for implementing a cache coherency system with each cache line having a respective tag address that identifies associated data and each cache line having state information that indicates a state of the associated data for the respective cache line was well known as evidenced by Cypher, an artisan would have been motivated to implement this feature in the system of Arimilli and Chen in order to specify the access rights and ownership responsibilities for a corresponding processor. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Arimilli and Chen to include each cache line having a respective tag address that identifies associated data and each cache line having state information that indicates a state of the associated data for the respective cache line since this would have enabled specifying the access rights and ownership

responsibilities for a corresponding processor (col. 1, ll 23-25) as taught by Cypher.

As per claim 20, the rationale in the rejection of claim 11 is herein incorporated.

As per claim 21, the rationale in the rejection of claims 1 and 11 is herein incorporated.

As per claim 22, Chen discloses the source processor further comprises an associated source processor cache having a source processor cache line for storing the data, the source processor cache line having an associated state, the source processor storing the data in the source processor cache line and assigning a shared state to the associated state of the source processor cache line in response to receiving the S-DATA response from the target processor [coll6, ll 58 to col. 7, ll 17; col. 7, ll 49 to col. 8, ll 3].

As per claim 23, Chen discloses the source processor further comprises an associated source processor cache having a source processor cache line for storing the data, the source processor cache line having an associated state, the source processor storing the data in the source processor cache line and assigning a dirty state to the associated state of the source processor cache line in response to receiving the D-DATA response from the target processor [col. 7, ll 49-61; col. 8, ll 52-67].

Allowable Subject Matter

7. Claims 2-7, 13-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. The examiner requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line no(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

10. When responding to this office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections See 37 CFR 1.111 (c).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mardochee Chery whose telephone number is (571) 272-4246. The examiner can normally be reached on 8:30A-5:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sough Hyung can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

April 13, 2007

HYUNG SOUGH
SUPERVISORY PATENT EXAMINER
4-16-07

Mardochee Chery
Examiner